REMARKS

In section 2 of the Office Action, the Examiner objected to the drawings as failing to show a capacitive switching ratio greater than 20. The Examiner has misinterpreted Figure 4 and the specification. As disclosed in the specification, Figure 4 shows a capacitive switching ratio for the varactor 10 that is on the order of 33. Thus, as shown in Figure 4, C_{max} is on the order of 33 pf and C_{min} is on the order of 1 pf. Accordingly, the drawings show a capacitive switching ratio that is greater than 20.

In section 3 of the Office Action, the Examiner has objected to the specification for the same reasons. However, as explained above, and as disclosed in the specification, Figure 4 shows a capacitive switching ratio for the varactor 10 that is on the order of 33. Thus, as shown in Figure 4, C_{max} is on the order of 33 pf and C_{min} is on the order of 1 pf. Accordingly, the specification and the drawings are consistent.

In section 4 of the Office Action, the Examiner has objected to claim 40 for the same reasons. However, as explained above, and as disclosed in the specification, Figure 4 shows a capacitive switching

ratio for the varactor 10 that is on the order of 33. Thus, as shown in Figure 4, C_{max} is on the order of 33 pf and C_{min} is on the order of 1 pf. Accordingly, claim 40 is consistent with the specification and the drawings.

In section 6 of the Office Action, the Examiner rejected claims 32-40 under 35 U.S.C. §103(a) as being unpatentable over the Chiang patent in view of the Litwin patent.

The Chiang patent discloses a varactor 31 in Figure 1. The varactor 31 has an active semiconductor layer 32 which is sandwiched between a dielectric 33 and an n-type ground electrode 34. A gate electrode 35 is deposited on top of the dielectric film 33. (It is noted that, based upon the text of the Chiang patent, the reference numeral 33 should point to the layer denoted by t_d and the reference numeral 32 should point to the layer denoted by t_{si}.) The varactor 31 includes an insulating substrate 36, and the ground electrode 34 sits on the insulating substrate 36.

The varactor 31 is switched back and forth between its maximum capacitance accumulation mode and its minimum capacitance depletion mode by reversing the polarity of its gate voltage Vg. Whenever the gate 35 of the varactor 31 is positively biased, electrons are

accumulated in the silicon layer 32 near its interface with the dielectric film 33. Conversely, when the gate 35 is sufficiently negatively biased, the silicon layer 32 is depleted of electrons.

The Chiang patent states that, if the active silicon layer 32 is single crystal silicon, capacitive switching ratios R well in excess of two can be achieved. However, according to the Chiang patent, existing single crystal silicon technology is not applicable to the fabrication of large area integrated circuits, and it is difficult to obtain high capacitive switching ratios R for the varactor 31 if its active semiconductor layer 32 is composed of amorphous silicon.

The Chiang patent also discloses a varactor 41 in Figures 2 and 3. The varactor 41 has smaller effective capacitive surface areas in depletion than in accumulation, and the varactor 41 uses poly-silicon thin films. The varactor 41 has a ground layer 42 of undoped or very lightly doped silicon on a thick insulating substrate 43. A thin dielectric film 44 is formed on the ground layer 42, and a metal or silicon p+ or n+ gate electrode 46 is deposited on the dielectric film 44.

N+ or p+ ground electrodes 45 are formed in the ground layer 42 so that they only partially and laterally

overlap the gate electrode 46. As a result, the gate electrode 46 longitudinally aligns with a section 47 of the active silicon layer 42 which is beyond the lateral edges of the ground electrodes 45, but which is in intimate electrical contact with the substrate 43. The extent to which the ground electrodes 45 laterally overlap the gate electrode 46 is determined by the lateral scattering of impurities during doping of the ground electrodes 45 as the impurities migrate into the silicon film 42.

The Chiang patent states that the capacitive switching ratio R for the varactor 41 is controlled by the ground-gate overlap. In other words, the capacitive switching ratio R for the varactor 41 is equal to the ratio of the length L of the gate to the ground overlap length $2L_2$. The Chiang patent further states that there is a performance tradeoff between switching speed and RF impedance on the one hand and capacitive switching ratio R on the other. Thus, switching speed can be increased and RF impedance can be lowered at the cost of decreased capacitive switching ratio R. Alternatively, the capacitive switching ratio R can be increased at the cost of decreased switching speed and increased RF impedance.

A varactor 51 as shown in Figure 4 is a bottom-gate counterpart to the varactor 41.

Figures 5 and 6 show top-gate and bottom-gate varactors 61 and 62, respectively. The ground electrodes 45 of the varactors 61 and 62 reside in a suitably patterned conductive layer 63 which is physically distinct from the active silicon film 42, but which is in intimate contact therewith in partially overlapping alignment with the gate electrode 46. Again, the capacitive switching ratios R for the varactors 61 and 62 are controlled by their respective ground-gate overlaps.

A top-gate varactor 71 shown in Figures 7 and 8 has gate electrode segments 46a-46m and ground electrode segments 45a-45n which are laterally staggered with respect to the gate electrode segments 46a-46n, where n = m + 1. Each of the gate electrode segments 46a-46m is partially and laterally overlapped by two of the ground electrode segments 46a-46n such that neighboring gate electrode segments share the ground electrode segments that are disposed between them. Accordingly, each of the intermediate ground electrode segments partially overlaps the gate electrode segments to its immediate right and left. The gate electrode segments 46a-46m are

electrically interconnected, and the ground electrode segments 45a-45n are electrically interconnected.

Figure 9 illustrates a varactor 81 which is a bottom-gate counterpart to the varactor 71.

Independent claim 32 - The Examiner recognizes that the Chiang patent does not disclose a varactor having a plurality of alternating P- type wells and N+ type regions in a silicon layer. Therefore, the Examiner relies on Figure 2 of the Litwin patent which shows a varactor 20 having n+ type source and drain regions and a p type well. The Examiner then argues that, because lightly doped well regions are desirable as evidenced by the Litwin patent, it would have been obvious to incorporate such lightly doped well regions in the varactors disclosed in the Chiang patent to form varactors having a plurality of alternating P- type wells and N+ type regions in a silicon layer.

However, there are a number of problems with this argument.

First, the Examiner argues that the particular combination of the Chiang patent and the Litwin patent as espoused by the Examiner is desirable, but the Examiner does not explain what would make this combination desirable to one of ordinary skill in the art. The

argument that this combination is desirable is merely a conclusion. The Examiner has failed to explain why such a combination is desirable. Therefore, the Examiner has not made out a prima facie case of obviousness.

Accordingly, for this first reason, independent claim 32 is not obvious over the Chiang patent in view of the Litwin patent.

Second, the Litwin patent in Figure 2 discloses n+ source and drain regions 23 and 24 formed in a p-type well 22. The nomenclature (p instead of p+ or p-) as used in Figure 2 indicates that the well 22 is moderately doped (p) instead of lightly doped (p-).

Therefore, the Litwin patent does not suggest a varactor with alternating p- wells and n+ regions.

The Chiang patent discloses that the silicon 42 can be undoped or light doped. However, the Chiang patent does not disclose or suggest whether, if the silicon film 42 is to be lightly doped, the silicon 42 should be lightly doped with p-type impurities to produce p- regions. Moreover, the Chiang patent does not disclose or suggest whether, if the silicon film 42 is to be lightly doped, the silicon 42 should be doped so as produce alternating lightly doped p- regions and heavily doped n+ regions.

Accordingly, neither the Litwin patent nor the Chiang patent discloses or suggests forming a varactor by lightly doping the silicon 42 with p-type impurities to produce p- regions and heavily doping the silicon 42 with n-type impurities to produce n+ regions.

Accordingly, for this second reason, independent claim 32 is not obvious over the Chiang patent in view of the Litwin patent.

Third, the Chiang patent discloses that its varactor is intended for large area integrated circuits. Also, the dashed lines in Figure 2 of the Chiang patent seem to suggest that the electrode 45 are doped down to the dielectric layer 43.

The Litwin patent, on the other hand, discloses in column 7, lines 18-32 that, in the case where its varactors are integrated with other devices (thereby producing an integrated circuit), the source and drain regions need to be formed in a well region.

Therefore, because of these conflicting disclosures, the Litwin patent suggests that it cannot be combined with the Chiang patent so as to meet the limitations of independent claim 32.

Accordingly, for this third reason, independent claim 32 is not obvious over the Chiang patent in view of the Litwin patent.

Fourth, the Chiang patent discloses that the capacitive switching ratio R of its varactor is dependent on the gate-ground overlap ratio. Thus, the Chiang patent discloses that the capacitive switching ratio R can be increased by increasing gate length versus ground overlap length.

On the other hand, the Litwin patent discloses that the capacitive switching ratio R (referred to in the Litwin patent as dynamic range) of its varactor can be made high by making the well as lightly doped as possible at its principle surface region (i.e., under the gate 36 and near the insulating layer 25). Indeed, the Litwin patent discloses that additional doping of the well should be blocked. Thus, the well region 22 starts out as a moderately doped region, as indicated by the p notation in Figure 2. The Litwin patent then discloses that the well region 22 should receive little additional doping.

Accordingly, the Chiang patent and the Litwin patent suggests solutions to increasing the capacitive switching ratio R that are not compatible.

Consequently, one of ordinary skill in the art would not combine the Chiang patent and the Litwin patent as suggested by the Examiner so as to meet the limitations of independent claim.

Therefore, for this fourth reason, independent claim 32 is not obvious over the Chiang patent in view of the Litwin patent.

Because independent claim 32 is patentable over the Chiang patent in view of the Litwin patent, dependent claims 33-40 are similarly patentable over the Chiang patent in view of the Litwin patent.

Moreover, dependent claim 34 requires the SOI structure recited in independent claim 32 to include a layer of high resistivity silicon under the insulation layer. The Litwin patent does not disclose an SOI structure, and the Chiang patent does not disclose that the insulating layer 43 is over a silicon layer or that such a silicon layer is high resistivity silicon. Accordingly, the combination of the Chiang patent and the Litwin patent does not disclose or suggest the invention of dependent claim 34.

The Examiner contends that it is well known that silicon handle layers below the insulating layers of SOI structures are highly resistive. However, the

Examiner has not shown that it would have been obvious to provide the Chiang/Litwin varactor in an SOI structure having a highly resistive silicon substrate. The Examiner has only argued that SOI structures with highly resistive silicon substrate are known.

Accordingly, the Examiner has not made out a prima facie case of obviousness with respect to dependent claim 34.

Therefore, dependent claim 34 is not obvious over the Chiang patent in view of the Litwin patent.

Dependent claim 37 recites that the P- wells form a transistor body, and that the transistor body is allowed to float. Neither the Chiang patent nor the Litwin patent discloses or suggests this feature. Accordingly, the combination of the Chiang patent and the Litwin patent does not disclose or suggest the invention of dependent claim 37.

The Examiner makes no contentions or arguments with respect to dependent claim 37.

Therefore, dependent claim 37 is not obvious over the Chiang patent in view of the Litwin patent.

Dependent claims 39 and 40 recite that the capacitive switching ratio is equal to or greater than 5 and 20, respectively. The only capacitive switching

ratio mentioned in the Chiang patent is greater than 2, and the Litwin patent does not mention any specific capacitive switching ratios.

The Examiner argues that a high capacitive switching ratio is desirable. However, neither the Chiang patent nor the Litwin patent disclose how to achieve a capacitive switching ratio equal to or greater than 5.

The Examiner also argues that the gate width to gate length ratios given in the Litwin patent at column 6, lines 10-17 are similar to those given in the present application. The Examiner, however, has not demonstrated (i) what specific gate and width lengths from the Litwin patent produce the same gate width to gate length ratios as disclosed in the present application, (ii) why these gate width to gate length ratios are even pertinent to capacitance switching ratios, and (ii) that the number of gates disclosed in either the Chiang pate or the Litwin patent will produce the claimed capacitance switching ratios.

Therefore, dependent claims 39 and 40 are not obvious over the Chiang patent in view of the Litwin patent.

CONCLUSION

In view of the above, the claims of the present application are definite and patentably distinguish over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the present application are respectfully requested.

Respectfully submitted,

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